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- ITO Pattern (MASK5)
- ITO Sputtering
- Passivation Etch (MASK4)
- SINx PECVD
- n+ a-Si Etch-Back
- S/D Pattern (MASK3)
- S/D Sputtering
- a-Si Pattern (MASK2)
- n+ a-Si/a-Si/SINx PECVD
- Gate Pattern (MASK 1)
- Gate Metal Sputtering

300

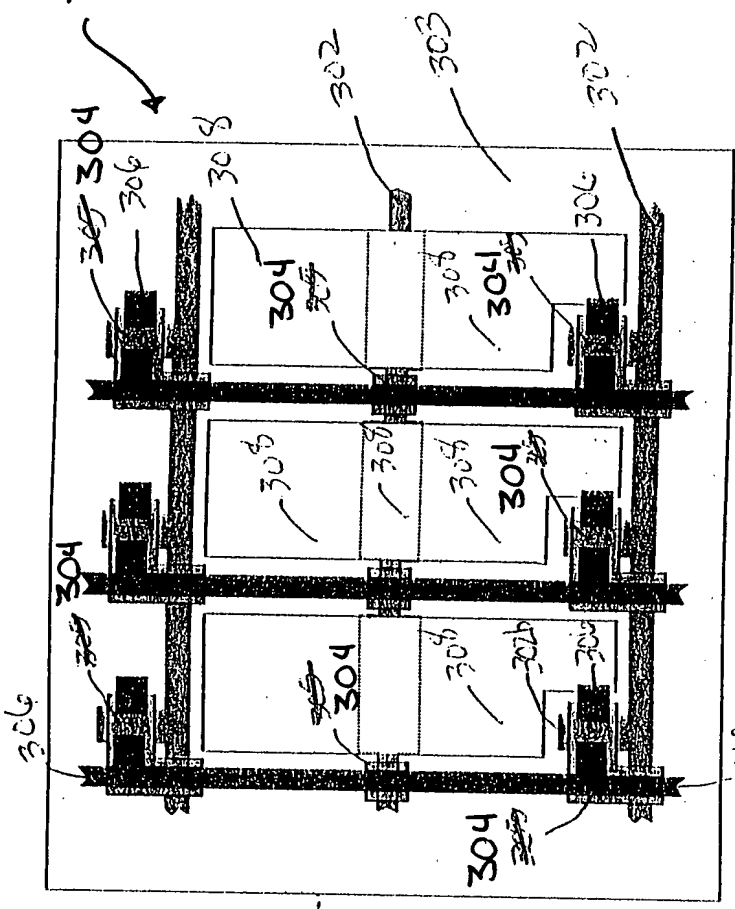


Fig. 3C

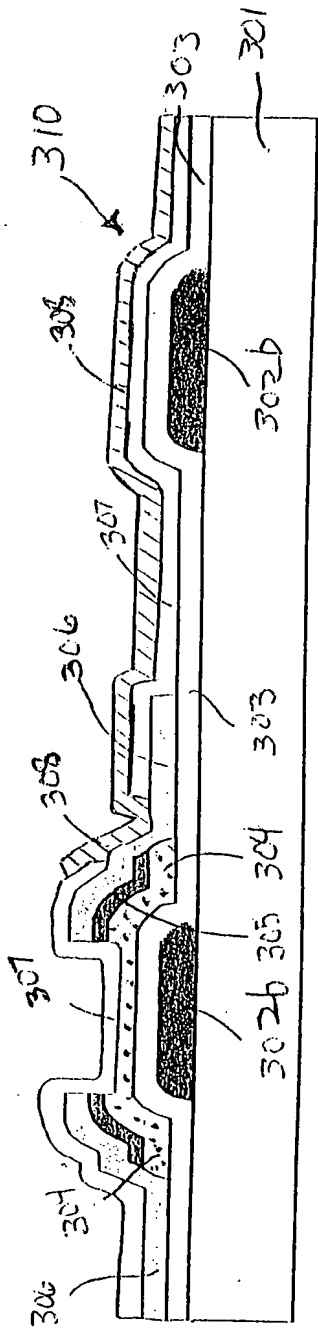


Fig. 3A

Fig. 3B